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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,444	10/11/2001	Ching-Te Lin	TI-31518	9172
23494	7590	03/15/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED			PHAM, LONG	
P O BOX 655474, M/S 3999			ART UNIT	
DALLAS, TX 75265			PAPER NUMBER	
			2814	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/975,444

Applicant(s)

LIN ET AL.

Examiner

Long Pham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12-16 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 12-16 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Rejections and/or objections as previously applied

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. Claims 12, 13, 14, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Iacoponi et al. (US '754) and Chen et al. (US 6,140,227).

AAPA teaches a method of fabricating an integrated circuit, comprising the steps of (see figure 1 and the background of the Invention on pages 1 and 2):

forming a dielectric layer over a semiconductor body;
forming a trench 12 in a first part of said dielectric layer;
depositing a liner/barrier material 14 over said dielectric layer including said trench using physical vapor deposition;
depositing a seed layer 16 over said liner/barrier layer; and
depositing a copper layer over said seed layer.

AAPA fails to teach sputter etching the barrier layer using a low bias before the seed layer is formed over the trench as recited in present claim 12.

Chen et al. teach forming a dielectric layer 204 having a trench over a semiconductor body 200, depositing a barrier layer 208 over the dielectric layer including the trench, and sputter etching a part or an overhang portion of the barrier layer before forming a conductive layer 212 to prevent voids inside the formed conductive layer. See figs. 2A-2C, related text, and col. 3, lines 20-30.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to sputter etch the barrier layer or an overhang portion of

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the barrier layer before the formation of a conductive layer or a layer for forming a conductive layer in the process of AAPA to obtain the above advantage.

AAPA further fails to teach that a via is formed in the dielectric layer as recited in present claim 12.

Iacoponi et al. teach a dielectric layer 116,108 having a trench and a via 118, 106 to enable metallization. See col. 1, lines 20-35.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to include a via in the dielectric layer in the process of AAPA to achieve the above benefit.

With respect to claim 15, the use of Ti, Tin, Ta, or TaN is well-known to one of ordinary skill in the art of making semiconductor devices.

Chen et al. fail to teach that the sputter etching is done at low voltage or low bias or at a voltage of 0 to -300 volts as recited in present claim 16.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal range for the sputtering bias or voltage through routine experimentation and optimization to obtain optimal or desired device performance because the sputtering bias or voltage is a result-effective variable and there is no evidence indicating that the sputtering bias or voltage is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Response to Arguments

3. Applicant's arguments filed 12/07/04 have been fully considered but they are not persuasive. See below.

In response to the applicants' arguments in the paragraph on page 4 of the Amendment dated 12/07/04, it is submitted that AAPA in view of Iacoponi et al. and Chen et al. teaches the claimed invention. See the above rejection.

Further, It is submitted that AAPA teaches the bi-layer barrier and Chen et al. is being relied on only for the teaching of sputtering etching a barrier layer after its formation.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

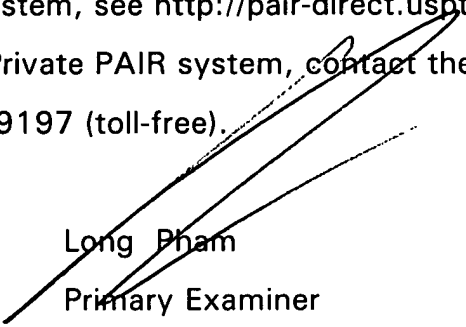
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Long Pham
Primary Examiner
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LP